REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Change to section 1.6 Added RAMP2s parameter to Table IA. - ksr	09-05-07	Joseph Rodenbeck
B	Updated drawing to meet current MIL-PRF-38535 requirements. Removed class M references. Updated Figure 4 to reflect vendor's current modeling and testing methods. Table IA changes to t_{AXQX}, t_{SHQZ}, t_{GLQX}, t_{GHQZ}, t_{WLQZ}, t_{WHQX}, C_{IN}, and C_{OUT}. Update Table IB in accordance with current vendor testing methods. - glg	14-03-06	Charles Saffle
C	Section 1.6 corrections to dose rate induced upset and survivability parameters. Table IA, corrections to t_{WLWH} and t_{PHWH} parameters. - glg	15-07-14	Charles Saffle
D	5 year review and update to current boilerplate as result of 5 YR review. - krw	22-03-14	James Eschmeyer

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

Revision Status of Sheets

REV	D	D	D																			
SHEET	23	24	25																			
REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

PREPARED BY
Kenneth Rice

CHECKED BY
Rajesh Pithadia

APPROVED BY
Raymond Monnin

DRAWING APPROVAL DATE
06-07-18

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/LandandMaritime

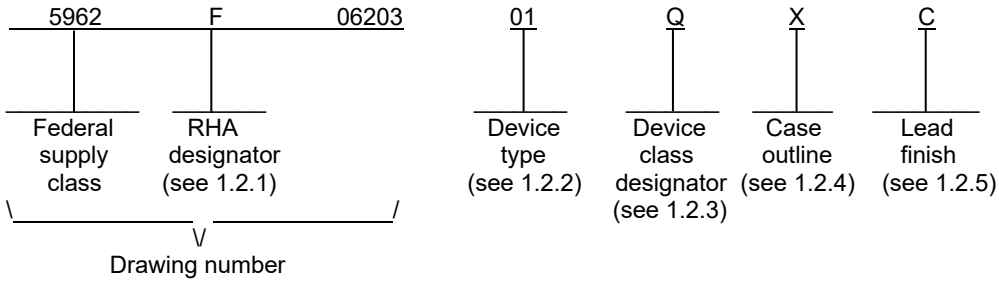
MICROCIRCUIT, MEMORY, DIGITAL, CMOS/SOI, RADIATION-HARDENED, 512K x 8-BIT, LOW VOLTAGE SRAM, MONOLITHIC SILICON

AMSC N/A	REVISION LEVEL D	SIZE A	CAGE CODE **67268**	**5962-06203**
		SHEET	1 OF 25	

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time	Sleep Mode
01	HX6408X_FN25	512K X 8-bit rad-hard CMOS/SOI SRAM 300 KRAD	25 ns	Non-Sleep
02	HX6408X_FN20	512K X 8-bit rad-hard CMOS/SOI SRAM 300 KRAD	20 ns	Non-Sleep
03	HX6408X_FM25	512K X 8-bit rad-hard CMOS/SOI SRAM 300 KRAD	25 ns	Sleep
04	HX6408X_FM20	512K X 8-bit rad-hard CMOS/SOI SRAM 300 KRAD	20 ns	Sleep
05	HX6408X_HN25	512K X 8-bit rad-hard CMOS/SOI SRAM 1 MRAD	25 ns	Non-Sleep

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q, V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style	Lid
X	See figure 1	36	Flat pack	gold/nickel metal

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38535 for classes Q and V.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{DD})	-0.5 V dc to +4.6 V dc
DC input voltage range (V_{IN})	-0.5 V dc to V_{DD} + 0.5 V dc
DC output voltage range (V_{OUT})	-0.5 V dc to V_{DD} + 0.5 V dc
DC or average output current (I_{OUT})	25 mA
Storage temperature	-65°C to +150°C
Lead temperature (soldering 5 seconds)	+270°C
Thermal resistance, junction to case (Θ_{JC})	2.0 °C/W
Output voltage applied to high Z-state	-0.5 V dc to V_{DD} + 0.5V dc
Maximum power dissipation	2.5 W
Operating free-air temperature, (T_A)	-55°C to +125°C
Maximum junction temperature (T_J)	175°C

1.4 Recommended operating conditions. 3/

Supply voltage range (V_{DD})	3.0 V dc to 3.6 V dc
Supply voltage reference (V_{SS})	0.0 V dc
High level input voltage range (V_{IH})	0.7 x V_{DD} to V_{DD} + 0.3 V dc
Low level input voltage range (V_{IL})	-0.3 V dc to 0.3 x V_{DD}
Voltage on any pin (V_{IN})	-0.3 V dc to V_{DD} + 0.3
Supply voltage ramp time (V_{DD} Ramp Time)	50 ms Maximum
Operating free-air temperature, (T_A)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	100 percent

1.6 Radiation features. 4/

Maximum total dose available (dose rate = 50-300 rad/s)	
Devices 01-04	300 KRads(Si)
Device 05	1 M Rads(Si)
Single event phenomenon (SEP).	
No SEL occurs at effective LET (see 4.4.4.4)	≤ 120 MeV-cm^2/mg
Heavy Ion Single event upset (SEU) rate	1 x 10^{-10} upsets/bit-day 5/
Proton Single event upset (SEU) rate	1 x 10^{-10} upsets/bit-day 5/
Neutron irradiation	1 x 10^{14} neutrons/cm^2 6/
Dose rate data upset	1 x 10^{10} Rad(Si)/sec for < 20 nsec
Dose rate survivability	1 x 10^{12} Rad(Si)/sec for < 20 nsec
Latch-up	Immune by SOI technology

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ All voltages are referenced to V_{SS}.

3/ Maximum applied voltage shall not exceed 4.6 V.

4/ For details on these RHA parameters and test results, contact the device manufacturer.

5/ Projected performance based on CREME96 results for a geosynchronous orbit during solar minimum non-flare conditions behind 100mil Aluminum shield using Weibull parameters derived from actual test data (see 4.4.4.4). Weibull parameters are available from the vendor to calculate upset rates for other orbits/environments (such as Adams 90% worst case) and using different upset rate calculating programs (such as Space Radiation 5.0).

6/ Guaranteed but not production tested.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil).

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

ASTM INTERNATIONAL (ASTM)

ASTM Standard F1192 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org.)

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD 78 - IC Latch-Up Test.

(Copies of these documents are available online at https://www.jedec.org.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see Appendix B to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and Figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on Figure 2.

3.2.3 Truth table. The truth table shall be as specified on Figure 3.

3.2.4 Output load circuit. The output load circuit for functional tests shall be as specified on Figure 4.

3.2.5 Tester timing characteristics and timing waveforms. The tester AC timing characteristics and timing waveforms shall be as specified on Figure 5 and applies to capacitance, read cycle, and write cycle measurements unless otherwise specified.

3.2.6 Radiation exposure circuit. The radiation test circuit shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request.

3.2.7 Functional tests. Various functional tests used to test this device are contained in the appendix A (herein). If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device classes Q and V, alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics. 1/ 2/

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $3.0\ V \le V_{DD} \le 3.6\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Standby Current – deselected, enabled	I_{DDSB2}	F=0 MHz, NCS, CE, NOE, NWE = V_{DD}	1, 3	All		5.0	mA
			2			10.0	
Standby Current – selected, enabled	I_{DDSB}	F=0MHz, NCS=V_{SS}, CE=V_{DD}	1, 3	All		5.0	mA
			2			10.0	
Operating Supply Current Deselected & Enabled, address bus at max frequency 3/	I_{DDOP3}	F=40MHz, NCS, CE, NOE, NWE = V_{DD}	1, 2, 3	All		24	mA
Operating Supply Current Deselected, write mode 3/	I_{DDOP1}	F = 1MHz, NCS, NOE = V_{DD} NWE vector controlled	1, 2, 3	All		1.5	mA
Operating Supply Current Sleep Mode	I_{DDOP2}	F = 1MHz, NSL=V_{SS}, NWE vector controlled	1, 2, 3	03, 04		200	µA
Operating Supply Current Selected, write mode low frequency 3/	I_{DDOPW1}	F=1MHz, NCS=V_{SS}, NOE=V_{DD}, NWE vector controlled	1, 2, 3	All		9	mA
Operating Supply Current Selected, write mode high frequency 3/	$I_{DDOPW40}$	F=40MHz, NCS=V_{SS}, NOE=V_{DD}, NWE vector controlled	1, 2, 3	All		260	mA
Operating Supply Current Selected, read mode low frequency 3/	I_{DDOPR1}	F=1MHz, NCS=V_{SS}, NOE, NWE =V_{DD}	1, 2, 3	All		4.4	mA
Operating Supply Current Selected, read mode high frequency 3/	$I_{DDOPR40}$	F=40MHz, NCS=V_{SS}, NOE, NWE =V_{DD}	1, 2, 3	All		160	mA
Data Retention Current	I_{DR}	V_{DD} = 2.0 V	1, 2, 3	All		3	mA
Low level output voltage	V_{OL}	V_{DD} = 3.0 V, I_{OL}=10mA, V_{IL} = V_{SS}, V_{IH} = V_{DD}	1, 2, 3	All		0.4	V
High level output voltage	V_{OH}	V_{DD} = 3.0 V, I_{OH}=-5mA, V_{IL} = V_{SS}, V_{IH} = V_{DD}	1, 2, 3	All	2.7		V
Input leakage current	I_{ILK}	V_{IN} = 3.6 V, V_{DD} = 3.6 V, all other pins at 0.0 V	1, 2, 3	All		5	µA
Output leakage current	I_{OLK}	V_{OUT} = 3.6V, V_{DD} = 3.6 V, all other pins at 0.0 V	1, 2, 3	All		10	µA
V_{DD} Ramp rate functionality	RAMP50MS	Write and read March pattern to verify functionality after ramping V_{DD} from 0 V to 3.3 V in 50 ms with 50 mV steps	1, 2, 3	All			
V_{DD} Ramp rate functionality	RAMP2S	Write and read March pattern to verify functionality after ramping V_{DD} from 0 V to 3.3 V in 2 s with 50 mV steps	1, 2, 3	All			

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued. 1/ 2/

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $3.0\ V \le V_{DD} \le 3.6\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Input capacitance 4/	C_{IN}	$V_{IN} = V_{DD}$ or V_{SS}, f = 1 MHz	4	All		11	pF
Output capacitance 4/	C_{OUT}	See 4.4.1e	4	All		9	pF
Functional tests		See 3.2.7 and 4.4.1.c	7, 8	All			
Data retention voltage	V_{DR}	V_{DD} = 2.0 V	7, 8	All	5/		
Read cycle time	t_{AVAVR}	See figures 4 and 5; $V_{IH}=V_{DD}$, $V_{IL}=V_{SS}$	9, 10, 11	01,03,05	25		ns
				02, 04	20		
Address access time	t_{AVQV}		9, 10, 11	01,03,05		25	ns
				02, 04		20	
Address change output invalid time	t_{AXQX}		9, 10, 11	All	5		ns
Chip select access time	t_{SLQV}		9, 10, 11	01,03,05		25	ns
				02, 04		20	
Chip select to output enable time	t_{SLQX}		9, 10, 11	All	4		ns
Chip select to output disable time	t_{SHQZ}		9, 10, 11	All		4	ns
Output enable access time	t_{GLQV}		9, 10, 11	All		5	ns
Output enable to output active time	t_{GLQX}		9, 10, 11	All	0.4		ns
Output enable to output disable time	t_{GHQZ}		9, 10, 11	All		3	ns
Write cycle time	t_{AVAVW}		9, 10, 11	01,03,05	25		ns
				02, 04	20		
Minimum write enable pulse width	t_{WLWH}		9, 10, 11	01,03,05	25		ns
				02, 04	15		
Chip select to end of write time	t_{SLWH}		9, 10, 11	01,03,05	20		ns
				02, 04	16		
Data valid to end of write time	t_{DVWH}		9, 10, 11	01,03,05	15		ns
				02, 04	12		
Address valid to end of write time	t_{AVWH}		9, 10, 11	01,03,05	25		ns
				02, 04	20		
Data hold time after end of write time	t_{WHDX}		9, 10, 11	All	0		ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued. 1/ 2/

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $3.0\ V \le V_{DD} \le 3.6\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Address valid setup to start of write time	t_{AVWL}	See figures 4 and 5; $V_{IH}=V_{DD}$, $V_{IL}=V_{SS}$	9, 10, 11	All	0		ns
Address valid hold after end of write time	t_{WHAX}		9, 10, 11	All	0		ns
Write enable to output disable time	t_{WLQZ}		9, 10, 11	All		6	ns
Write disable to output enable time	t_{WHQX}		9, 10, 11	All	6		ns
Write disable write enable pulse width	t_{WHWL}		9, 10, 11	All	5		ns
Sleep disable output enable time	t_{PHQX}		9, 10, 11	03, 04	5		ns
Sleep disable access time	t_{PHQV}		9, 10, 11	03		25	ns
				04		20	
Sleep enable output disable time	t_{PLQZ}		9, 10, 11	03, 04		10	ns
Sleep disable to write high time	t_{PHWH}		9, 10, 11	03	25		ns
				04	25		

1/ Pre-irradiation values for RHA marked devices shall also be the post-irradiation values unless otherwise specified.
2/ When performing post-irradiation electrical measurements for any RHA level T_A = +25°C. Limits shown are guaranteed at T_A = +25°C ± 5°C.
3/ This dynamic operating mode current measurement (I_{DDOPx}) excludes standby mode current (I_{DDSB}).
4/ Tested initially and after any design or process changes which may affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
5/ As verified by functional tests.

TABLE IB. SEP Test Limits 1/ 2/

Device Type	Memory pattern	V_{DD} = 3.0 V SEU rate 4/ Adam 90% environment	Bias V_{DD} =3.6 V for latch-up (SEL)test No SEL occurs at effective LET = 5/
All	3/	1×10^{-10} upsets/bit-day	LET $\le$ 120 MeV-cm^2/mg

1/ For SEP test conditions, see 4.4.4.4 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Testing shall be performed using checkerboard and checkerboard bar test patterns.
4/ Based on CREME96 results for a geosynchronous orbit during solar minimum non-flare conditions behind 100mil Aluminum shield using Weibull parameters derived from actual test data (see 4.4.4.4). Weibull parameters are available from the vendor to calculate projected upset rates for other orbits/environments (such as Adams 90% worst case) and using different upset rate calculating programs (such as Space Radiation 5.0).
5/ Worst case temperature T_A = +125°C ± 10°C for SEL test.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA and IIB herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device classes Q and V, subgroups 7, 8A, and 8B shall include verifying the functionality of the device.

d. O/V (Latch-up) tests shall be measured only for the initial qualification and after any process or design changes which may affect the performance of the device. For device classes Q and V, the procedures and circuit shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JESD 78 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 5 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535.

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A, and as specified herein. The total dose requirements shall be as defined within paragraph 1.6 herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed in accordance with MIL-STD-883 method 1019 condition A and as specified herein. The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C.

4.4.4.2 Dose rate induced latch-up testing. When specified in the purchase order or contract, dose rate induced latch-up testing shall be performed in accordance with test method 1020 of MIL-STD-883 and as specified herein. Test shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. When specified in the purchase order or contract, dose rate upset testing shall be performed in accordance with method 1021 of MIL-STD-883 and herein.

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may affect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latch-up characteristics. Test four devices with zero failures. ASTM standard F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60 degrees to the normal, inclusive (i.e., 0° ≤ angled ≤ 60 degrees). No shadowing of the ion beam due to fixturing or package related effects are allowed.

b. The fluence shall be greater than 100 errors or ≥ 10^7 ions/cm2.

c. The flux shall be between 10^2 and 10^5 ion/cm^2/s. The cross section shall be verified to be flux independent by measuring the cross section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature +125°C.

f. Bias conditions shall be V_{DD}= 3.0 V dc for the upset measurements and V_{DD}= 3.6 V dc for the latchup measurements.

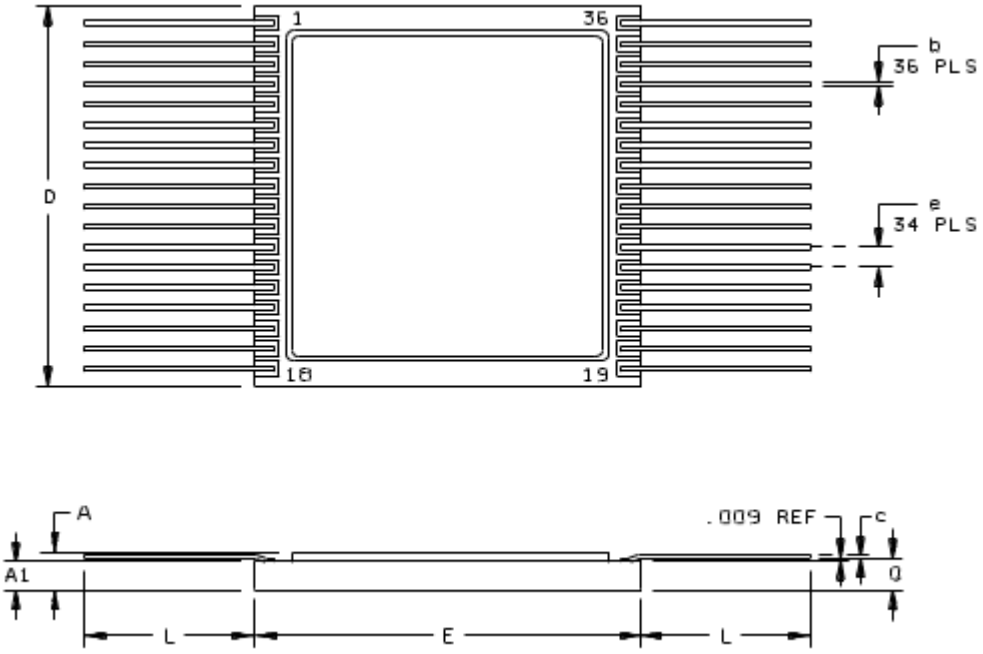
g. Test four devices with zero failures.

h. For SEP test limits see table IB herein.

4.4.4.5 Neutron testing. When required by the customer, neutron testing shall be performed in accordance with method 1017 of MIL-STD-883 and herein. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table IA, for the subgroups specified in table IIA herein at T_A = +25 ºC ±5 ºC after an exposure of 2 x 10^{14} neutrons/cm^2.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

Case outline X



Symbol	Millimeters			Inches		
	Min	Nom.	Max	Min	Nom.	Max
A	2.591	2.870	3.175	.102	.113	.125
A1	2.159	2.413	2.667	.085	.095	.105
b	.406	.457	.508	.016	.018	.020
c	.102	.152	.203	.004	.006	.008
D	23.11	23.37	23.62	.910	.920	.930
e	1.14	1.27	1.397	.045	.050	.055
E	21.133	21.336	21.539	.832	.840	.848
L		11.43			.450	
Q		2.642			.104	

NOTES:
1. The U.S. Government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
2. All exposed metalized areas are gold plated over electroplated nickel.
3. Package lid is electrically connected to V_{SS} for package X.

FIGURE 1. Case outline.

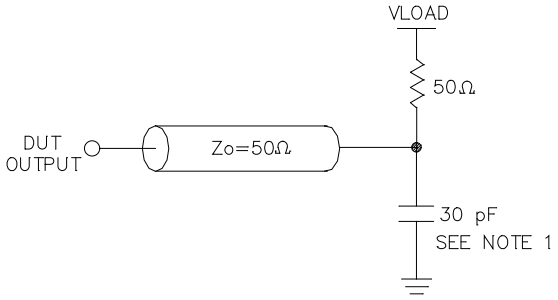
Device types	All
Case outlines	X
Terminal number	Terminal symbol
1	A0(CA2)
2	A1(CA0)
3	A2(CA3)
4	A3(CA5)
5	A4(CA7)
6	NCS
7	D0
8	D1
9	V_{DD}
10	V_{SS}
11	D2
12	D3
13	NWE
14	A5(CA4)
15	A6(CA6)
16	A7(RA10)
17	A8(RA0)
18	A9(RA1)
19	NC(NAS)
20	A10(RA8)
21	A11(RA5)
22	A12(RA7)
23	A13(RA9)
24	A14(RA6)
25	D7
26	D6
27	V_{DD}
28	V_{SS}
29	D5
30	D4
31	NOE
32	A15(RA3)
33	A16(RA2)
34	A17(RA4)
35	A18(CA1)
36	NSL

FIGURE 2. Terminal connections.

NCS	NSL	NWE	NOE	NAS	MODE	DQ
L	H	H	L	X	READ	Data Out
L	H	L	X	X	WRITE	Data In
H	X	X	X	X	Deselected	High Z
X	L	X	X	X	Disabled	High Z

Note : L=low, H=high, X=low or high

FIGURE 3. Truth table.

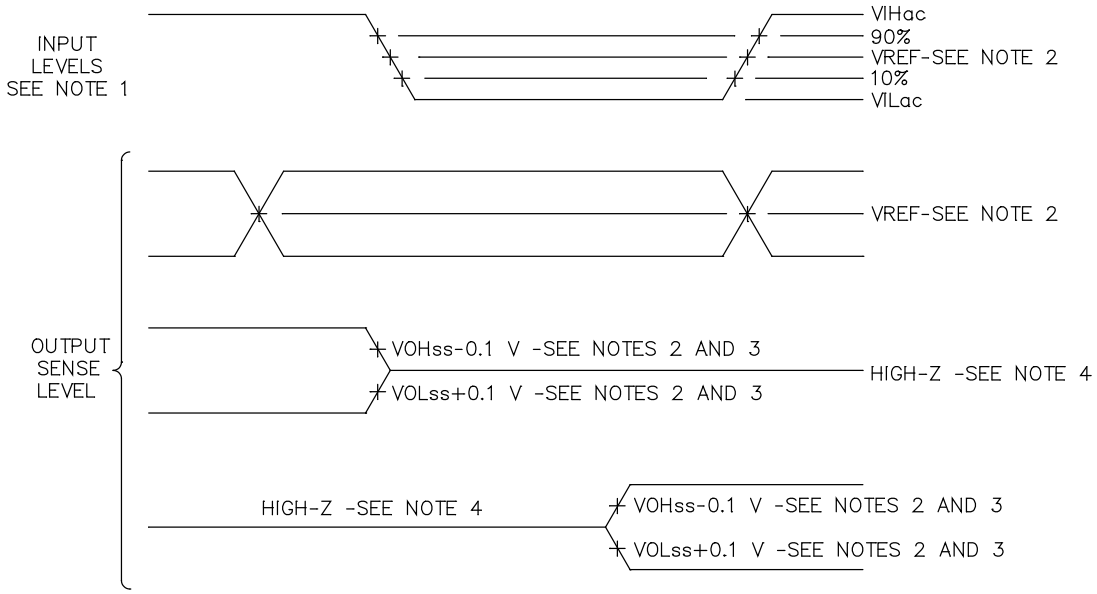


NOTE 1: Set to 5 pF for T*QZ (Low-Z to High-Z) timing parameters.

I/O Type	VLOAD
3.3V CMOS	VDDIO/2

FIGURE 4. Output load circuit

AC Timing Input and Output References



NOTES:

1. All input rise and fall times = 1 ns between the 90% and 10% levels.
2. Timing parameter reference voltage level.
3. ss: Low-Z V_{OH} and V_{OL} steady state output voltage.
4. High-Z output pin pulled to V_{LOAD} by output load circuit.

I/O type	$V_{IH}ac$	$V_{IL}ac$	V_{REF}
3.3V CMOS	V_{DDIO}	V_{SS}	$V_{DDIO}/2$

FIGURE 5. Timing waveforms.

Read cycle timing waveform

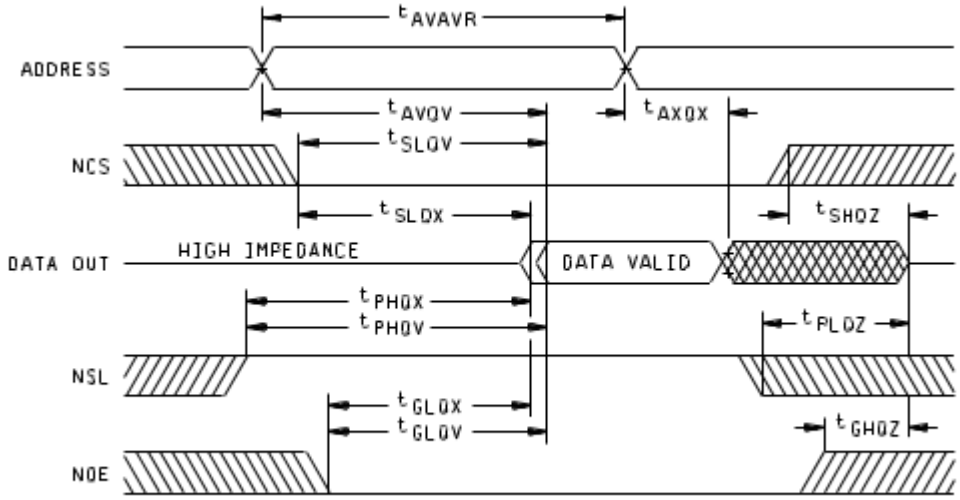


FIGURE 5. Timing waveforms - continued.

Write cycle timing waveform

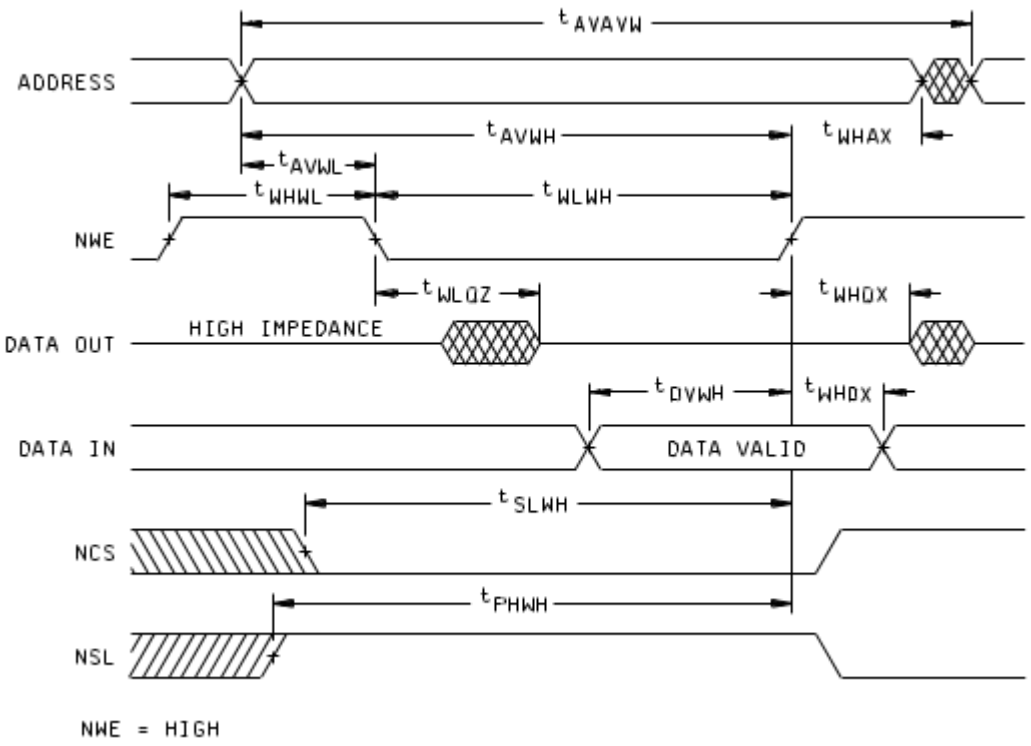


FIGURE 5. Timing waveforms - continued.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
2	Static burn-in (method 1015)	Not required	Required
3	Same as line 1		1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required
5	Same as line 1		1*, 7* Δ
6	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters (see 4.4)	2, 3, 8A, 8B	2, 3, 8A, 8B
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7, 8A, and 8B functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

Table IIB. Delta limits at +25°C.

Parameter 1/	Limits
I_{DDSB}	200 µA
I_{ILK}, I_{OLK}	1 µA

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal, or email communication.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0591.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions (SEP).

b. Number of upsets (SEU).

c. Number of transients (SET).

d. Occurrence of latch-up (SEL).

APPENDIX A

Appendix A forms a part of SMD 5962-06203

FUNCTIONAL ALGORITHMS

A.1 SCOPE

A.1.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

A.1.1.1 Functional Test Conditions. V_{IH} and V_{IL} levels during functional testing shall comply with the requirements of 3.2.7 herein.

A.1.1.2 Functional Test Sequence. Functional test patterns may be performed in any order.

A.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

A.3 ALGORITHMS

A.3.1 Algorithm A (pattern 1).

A.3.1.1 Checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

A.3.2 Algorithm B (pattern 2).

A.3.2.1 March Left-Right.
Step 1. Increment address from minimum to maximum writing each address with alternating data pattern (x55).
Step 2. Increment address from minimum to maximum while performing 2a and 2b.
Step 2a. Read and verify an address.
Step 2b. Write the address with complement data.
Step 3. Decrement address from maximum to minimum while performing 3a, 3b, 3c, 3d.
Step 3a. Read and verify an address.
Step 3b. Write the address with complement data.
Step 3c. Read and verify the address.
Step 3d. Write the address with complement data.
Step 4. Decrement address from maximum to minimum while performing 4a and 4b.
Step 4a. Read and verify the address.
Step 4b. Write the address with complement data.
Step 5. Decrement address from maximum to minimum while performing 5a, 5b, 5c, and 5d.
Step 5a. Read and verify the address.
Step 5b. Write the address with complement data.
Step 5c. Read and verify the address.
Step 5d. Write the address with complement data.
Step 6. Decrement address from maximum to minimum while performing 6a.
Step 6a. Read and verify the address.

A.3.3 Algorithm C (pattern 3).

A.3.3.1 Solids.

Step1. Write x55 data pattern to all addresses from minimum to maximum.
Step 2. Read and verify x55 data pattern at all addresses.
Step 3. Write xAA data pattern to all addresses from minimum to maximum.
Step 4. Read and verify xAA data pattern at all addresses.

A.3.4 Algorithm D (pattern 4).

A.3.4.1 Control Signals Functional Verfication.

Each test performed independently.
NOE Functional test: Read with NOE = V_{IH} and confirm high-Z outputs
NCS Functional test: Read with NCS = V_{IH} and verify high-Z outputs
NSL Functional test: Read with NSL = = V_{IL} and verify high-Z outputs

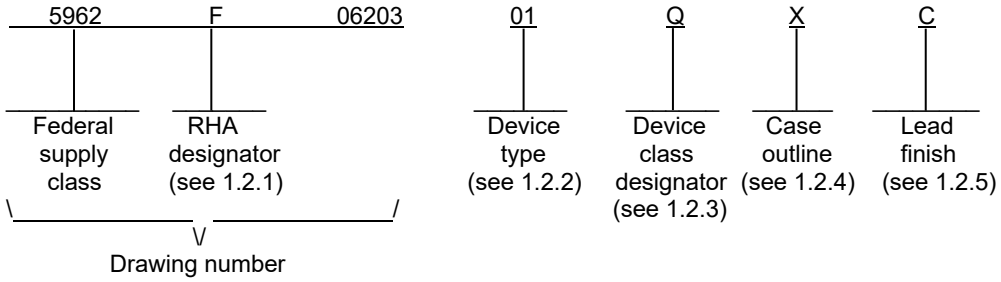
Appendix B

Appendix B forms a part of SMD 5962-06203

B.1 Scope

B.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QML plan for use in monolithic microcircuits, multichip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

B.1.2 PIN. The PIN is as shown in the following example:



B.1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

B.1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Circuit function	Access time
01	512K X 8 Rad-Hard CMOS/SOI SRAM	25 ns
02	512K X 8 Rad-Hard CMOS/SOI SRAM	20 ns

B.1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

B.1.2.4 Die code. The die code designator shall be a number 9 for all devices supplied as die only with no case outline.

B.1.2.5 Die details. The die details designation shall be a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

B.1.2.5.1 Die physical dimensions.

Device type	Die size	Die thickness	Die Detail	Figure Number
All	14492 µm X 14362 µm	675 ± 20 µm	A	B-1

B.1.2.5.2 Die bonding pad locations and electrical functions.

Device type	Die Detail	Figure Number
All	A	B-1

B.1.2.5.3 Interface materials

Device type	Top metallization	Backside metallization	Die Detail	Figure Number
All	Al/Cu, 9kÅ - 11.0 kÅ	None (backgrind)	A	B-1

B.1.2.5.4 Assembly related information.

Device type	Glassivation	Die Detail	Figure Number
All	Nitride 9kÅ	A	B-1

B.1.2.5.5 Wafer fabrication source.

Device type	Source	Die Detail	Figure Number
All	Honeywell SSEC, Plymouth	A	B-1

B.1.3 Absolute maximum ratings. See paragraph 1.3 within the body of this drawing for details.

B.1.4 Recommended operating conditions. See paragraph 1.4 within the body of this drawing for details.

B.2. APPLICABLE DOCUMENTS.

B.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK - 103 - List of Standard Microcircuit Drawings
MIL-HDBK - 780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil).

B.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

B.3. REQUIREMENTS.

B.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit or function as described herein.

B.3.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.

B.3.2.1 Die physical dimensions. The die physical dimensions shall be specified in B.1.2.5.1 and on figure B-1.

B.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in B.1.2.5.2 and on figure A-1. Bond pads may contain stub bonds that require compound bonding.

B.3.2.2.1 Additional die pads bonding instructions. The die contains a number of bonding pads for functions not pinned out in the single chip package configuration. The purchaser should contact the manufacturer for specific instructions for each application. The following paragraphs describe these additional functions. Failure to bond these functions appropriately may result in incorrect operation of the device.

B.3.2.2.1.1 Not address strobe (NAS). For synchronous options only, the falling edge of this signal strobes in new addresses and data. NAS should be bonded to V_{SS}.

B.3.2.2.1.2 Synchronous (SYNCH). SYNCH enables NAS during synchronous operation. SYNCH should be bonded to V_{SS}.

B.3.2.2.1.3 Chip enable, Chip enable address 0, Not Chip Enable Polarity0, Chip Enable Address 1, and Not Chip Enable Polarity 1. (CE, CEA0, NCEP0, CEA1, and NCE01). All of these signals support multi-chip module operation. In a single chip configuration CE, CEA0, and CEA1 shall be tied to V_{DD}. NCEP0 and NCEP1 shall be bonded to V_{SS}.

B.3.2.2.1.4 Slew Rate 1 and Slew Rate 2 (SR1, and SR2). SR1 and SR2 control the slew rate of the output buffers. The maximum slew rate is attained with the two signals bonded to V_{DD}.

B.3.2.2.1.5 Back Side Contact (BSC). These pads allow contact to the substrate of the die and shall be bonded to V_{SS}.

B.3.2.2.1.6 Disable Time Option (DTO). DTO is used for diagnostic purposes at wafer evaluation. DTO is bonded to V_{SS}.

B.3.2.2.1.7 Sleep Mode (NSL). NSL is used to enable sleep mode and shall be bonded to V_{DD} when not used

B.3.2.3 Interface materials. The interface materials for the die shall be as specified in B.1.2.5.3 and on figure A-1.

B.3.2.4 Assembly related information. The assembly related information shall be as specified in B.1.2.5.4 and figure B-1. Bond pads may contain stub bonds that require compound bonding.

B.3.2.5 Truth table. Where technically applicable, (for die) the truth table(s) shall be as defined within paragraph 3.2.3 of the body of this document.

B.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

B.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

B.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in B.1.2 herein. The certification mark shall be "QML" or "Q" as required by MIL-PRF-38535.

B.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see B.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

B.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

B.4. VERIFICATION

B.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

B.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum it shall consist of:

a. Wafer lot acceptance for Class V product using the criteria within MIL-STD-883 method 5007.

b. 100% wafer probe (see paragraph B.3.4)

c. 100% internal visual inspection to the applicable class Q or V criteria defined within MIL-STD-883 method 2010 or the alternate procedures allowed within MIL-STD-883 method 5004.

B.4.3 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed including groups A, B, C, D and E inspections and as specified herein except where MIL-PRF-38535 permits alternate in-line control testing.

B.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see B.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified within paragraphs 4.4.4, 4.4.4.1, 4.4.4.1.1, 4.4.4.2, 4.4.4.3, and 4.4.4.4.

B.5. DIE CARRIER

B.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

B.6 NOTES

B.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit application (original equipment), design applications and logistics purposes.

B.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime-VA, Columbus, Ohio, 43218-3990 or telephone (614) 692-0591.

B.6.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined within MILPRF-38535 and MIL-HDBK-1331.

B.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see B.3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

4 MEG - HX6408

CHIP SIZE (after saw)	14492µm	14362µm
CHIP SIZE*	14520µm	14390µm
Lower Left*	-7246µm	-7181µm
Upper Right*	7246µm	7181µm

* Saw Center to Saw Center (not including PM bar)

PAD LIST	X(µm)	Y(µm)	Signal (relative to center of sawed die)
1	-7076.45	6567.1	V_{SS}
2	-7076.45	6278.1	V_{DD}
3	-7076.45	5400.4	CA5
4	-7076.45	4988.6	CA6
5	-7076.45	4577.2	CA7
6	-7076.45	4165.7	RA10
7	-7076.45	3754.3	CA4
8	-7076.45	3415.5	NAS
9	-7076.45	3126.5	V_{DD}
10	-7076.45	2837.5	V_{SS}
11	-7076.45	2488.25	SYNCH
12	-7076.45	2074.1	NWE
13	-7076.45	1670.9	RA0
14	-7076.45	1267.7	RA1
15	-7076.45	864.5	RA9
16	-7076.45	461.3	RA8
17	-7076.45	172.3	RA7 (#1)
18	-7076.45	-276.4	V_{DD}
19	-7076.45	-565.4	V_{SS}
20	-7076.45	-976.9	RA7 (#2)
21	-7076.45	-1265.9	V_{SS}
22	-7076.45	-1554.9	V_{DD}
23	-7076.45	-1962.1	RA6
24	-7076.45	-2365.3	RA5
25	-7076.45	-2768.5	RA4
26	-7076.45	-3171.7	RA3
27	-7076.45	-3574.9	RA2
28	-7076.45	-3863.9	V_{SS}
29	-7076.45	-4152.9	V_{DD}
30	-7076.45	-4506.5	CE
31	-7076.45	-4856	CEA0
32	-7076.45	-5205.5	NCEP0
33	-7076.45	-5555	CEA1
34	-7076.45	-5904.5	NCEP1
35	-7076.45	-6193.5	BSC
36	-7076.45	-6482.5	V_{DD}
37	-7076.45	-6771.5	V_{SS}
38	7081.45	-6840.7	V_{SS}
39	7081.45	-6551.7	V_{DD}
40	7081.45	-6262.7	BSC
41	7081.45	-5973.7	V_{SS}
42	7081.45	-5684.7	V_{DD}
43	7081.45	-5367.7	DQ7
44	7081.45	-4928.7	DQ6
45	7081.45	-4547.9	V_{DD}
46	7081.45	-4258.9	V_{SS}
47	7081.45	-3941.9	DQ5
48	7081.45	-3502.4	DQ4
49	7081.45	-3122.1	V_{SS}
50	7081.45	-2833.1	V_{DD}
51	7081.45	-2544.1	V_{DD}
52	7081.45	-2255.1	SR2
53	7081.45	-1966.1	SR1
54	7081.45	-1677.1	V_{SS}
55	7081.45	-1388.15	NOE
56	7081.45	-1035	NSLP
57	7081.45	-681.9	DTO
58	7081.45	-328.8	V_{SS}
59	7081.45	-39.8	V_{DD}
60	7081.45	380.5	CA1
61	7081.45	787.7	CA2
62	7081.45	1194.9	CA3
63	7081.45	1602.1	CA0
64	7081.45	2009.3	NCS
65	7081.45	2362.2	V_{DD}
66	7081.45	2651.2	V_{SS}
67	7081.45	2940.2	V_{DD}
68	7081.45	3229.2	V_{SS}
69	7081.45	3546.2	DQ0
70	7081.45	3985.7	DQ1
71	7081.45	4369.9	V_{DD}
72	7081.45	4658.9	V_{SS}
73	7081.45	4975.9	DQ2
74	7081.45	5415.4	DQ3
75	7081.45	5795.6	V_{DD}
76	7081.45	6084.6	V_{SS}
77	7081.45	6373.6	V_{DD}
78	7081.45	6662.6	V_{SS}

Note: Bond pads may contain stub bonds that require compound bonding.

Figure B-1. Bond Pad Locations and Functions for Devices.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 22-03-14

Approved sources of supply for SMD 5962-06203 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962F0620301QXC	34168	HX6408XQFN25
5962F0620301VXC	34168	HX6408XVFN25
5962F0620301Q9A	34168	HX6408KQFN25
5962F0620301V9A	34168	HX6408KVFN25
5962F0620302QXC	34168	HX6408XQFN20
5962F0620302VXC	34168	HX6408XVFN20
5962F0620302Q9A	34168	HX6408KQFN20
5962F0620302V9A	34168	HX6408KVFN20
5962F0620303QXC	34168	HX6408XQFM25
5962F0620303VXC	34168	HX6408XVFM25
5962F0620304QXC	3/	HX6408XQFM20
5962F0620304VXC	3/	HX6408XVFM20
5962H0620305QXC	34168	HX6408XQHM25
5962H0620305VXC	34168	HX6408XVHM25

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ No longer available from an approved source.

Vendor CAGE number	Vendor name and address
34168	Honeywell Inc. 12001 State Highway 55 Plymouth, MN 55441